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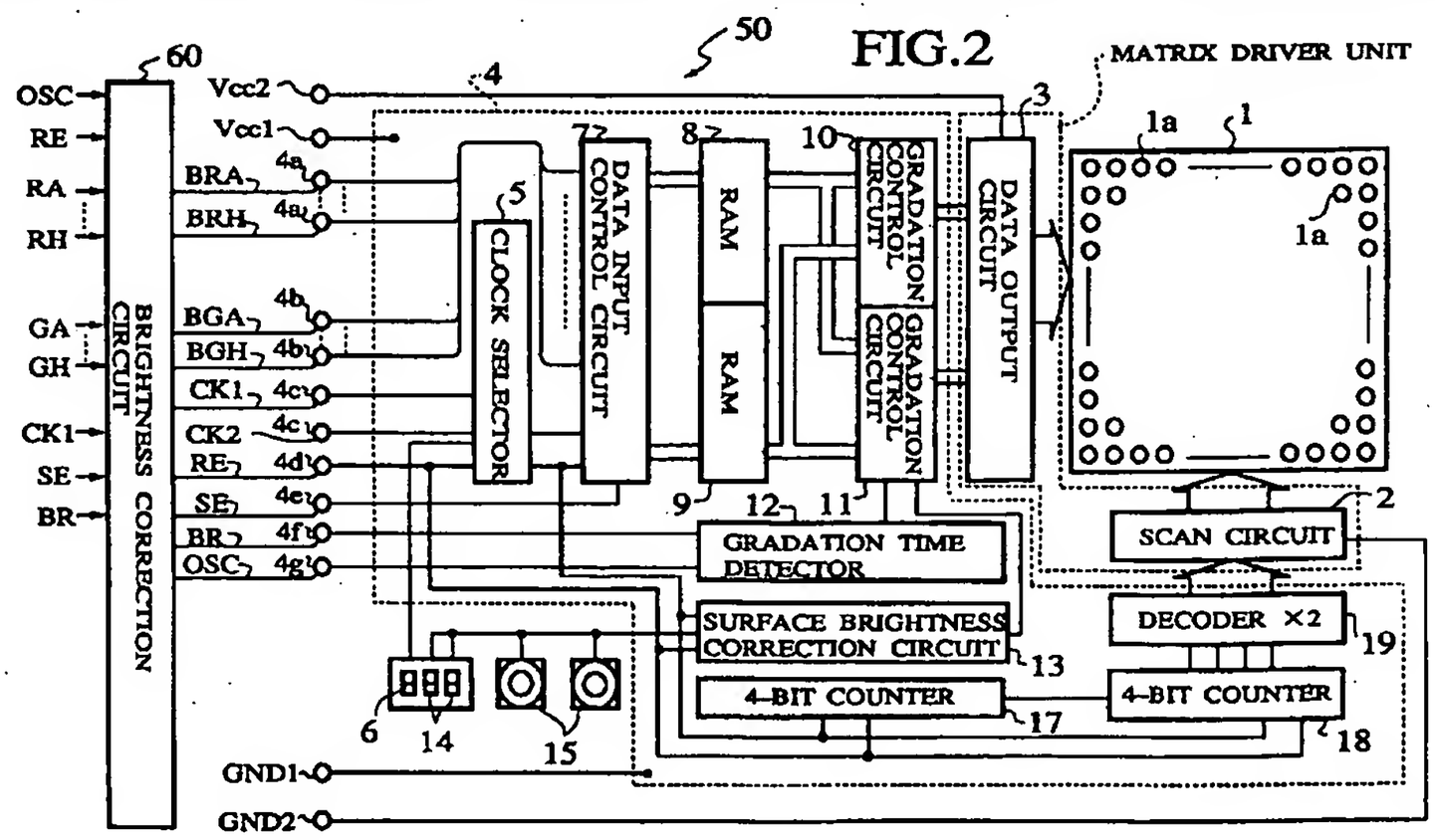
(54) Dot-matrix LED display and method of adjusting brightness of the same

(57) A dot-matrix LED display device has an LED array (1) with a dot matrix of LEDs (1a), a matrix driver unit (3) for driving the LEDs, and a control unit (4) for controlling the matrix driver unit. The display device has a data storage unit for storing brightness-corrected data prepared according to the characteristic brightness of each of the LEDs, selects the brightness-corrected data stored in the data storage unit according to externally provided display data, and drives the LEDs according to the selected brightness-corrected data. This arrangement minimizes brightness difference among the LEDs due to fluctuations in the characteristics of the LEDs.

FIG.2



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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a dot-matrix LED display device employing a matrix of LEDs (light emitting diodes) and a method of adjusting the brightness of the LEDs.

2. Description of the Prior Art

Dot-matrix LED display devices among other kinds of display device are relatively long life and easy to provide a large screen panel. Due to these advantages, they are widely used. Figure 1 is a block diagram showing a dot-matrix LED display device according to a prior art, employing red and green LEDs. An LED array 101 has a matrix of red and green LEDs 101a serving as dots. A scan circuit 102 sequentially scans the LEDs 101a. A data output circuit 103 drives the LEDs 101a in synchronization with the scan timing of the scan circuit 102. A control unit 104 controls the scan circuit 102 and data output circuit 103, to selectively light the LEDs 101a.

The control unit 104 receives, from the outside, 8-bit red display data RA to RH, 8-bit green display data GA to GH, clock signals CK1 and CK2, a reset signal RE, a select signal SE, a brightness signal BR, and an oscillation pulse OSC. In response to a control signal from a switch 106, a clock selector 105 selects the clock signal CK1 to achieve a one-phase clock mode or the clock signals CK1 and CK2 to achieve a two-phase clock mode. The output of the clock selector 105 is supplied to a data input control circuit 107, which is connected to a red and a green display data RAM 108, 109. The data input control circuit 107 receives the red and green display data in synchronization with the clock signal CK1 and stores them in the respective RAMs 108 and 109 according to the select signal SE. The outputs of the RAMs 108 and 109 are connected to red and green gradation control circuits 110 and 111, which are connected to the data output circuit 103.

The brightness signal BR adjusts a lighting time between pulses $CK1_n$ and $CK1_{n+1}$ of the clock signal CK1, where n = 32 x a, a being an integer among 1 to 32. A gradation time detector 112 receives the oscillation pulse OSC and calculates a gradation time by dividing the lighting time by 256. A surface brightness correction circuit 113 operates according to the clock signal CK1 and is controlled by an external switch 114 and an external brightness adjuster 115. Namely, the surface brightness correction circuit 113 provides data for correcting the total brightness of the display panel 101 according to a value set through the brightness adjuster 115. The gradation control circuits 110 and 111 refer to the gradation time provided by the gradation time detector 112 and the data provided by the surface brightness correction circuit 113 and controls the lighting time of each LED to display a color with one of 256 gradation levels according to the display data. The output of the clock selector 105 is also connected to two-stage 4-bit counters 117 and 118 connected in series. The outputs of the two-stage 4-bit counters 118 are connected to a decoder 119, which is connected to the scan circuit 102. The reset signal RE resets the clock selector 105, surface brightness correction circuit 113, and two-stage 4-bit counters 117 and 118.

The characteristics of the LEDs 101a differ from one another to cause brightness difference among them. To solve this problem, the prior art carries out selection work to equalize the characteristics of the LEDs 101a. This work increases the cost of a display device, in particular, a large-sized display panel comprising a plurality of the LED arrays.

SUMMARY OF THE INVENTION

To solve these problems, an object of the present invention is to provide a dot-matrix LED display device capable of realizing uniform brightness among LEDs and a method of adjusting the brightness of the display device. Another object of the present invention is to provide a dot-matrix LED display device having a simple structure capable of realizing uniform brightness among LEDs.

To achieve the objects, the present invention provides a dot-matrix LED display device shown in Fig. 2. The display device has an LED array 1 containing a matrix of LEDs; a matrix driver unit including a scan circuit 2 for driving the LEDs and a data output circuit 3; and a control unit 4 for controlling the matrix driver unit. What is characteristic to this display device is a brightness correction circuit 60 having a data storage unit for storing brightness-corrected data for each of the LEDs, to minimize brightness difference among the LEDs. The display device selects the brightness-corrected data according to externally provided display data RA to RH and GA to GH and determines the lighting time of each LED according to the selected brightness-corrected data, to thereby minimize brightness difference among the LEDs due to fluctuations in the characteristics of the LEDs.

Figure 3 shows the details of the brightness correction circuit 60. A ROM 69 stores the brightness-corrected data prepared for each of the LEDs to minimize brightness difference among the LEDs. A RAM 71 holds part of the brightness-corrected data of the ROM 69. When no display data is transferred from the outside, part of the brightness-corrected data is transferred from the ROM 69 to the RAM 71. When display data is externally provided, the brightness-corrected data in the RAM 71 is selected according to the display data, to drive the LEDs. Figure 7 is a time chart showing the operation of the brightness correction circuit 60, and Fig. 8 is a time chart showing the operation of the display device driven according to the brightness-corrected data. The data in the RAM is periodically refreshed, and the lighting time

of each LED is correctly determined according to the brightness-corrected data in the RAM, which operates at a high speed. This display device eliminates the work of selecting LEDs and is capable of minimizing brightness difference among LEDs at low cost and improving a displaying quality.

Other and further objects and features of the present invention will become obvious upon an understanding of the illustrative embodiments about to be described in connection with the accompanying drawings or will be indicated in the appended claims, and various advantages not referred to herein will occur to one skilled in the art upon employing of the invention in practice.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a dot-matrix LED display device according to a prior art;
Fig. 2 is a block diagram showing a dot-matrix LED display device according to an embodiment of the present invention;
Fig. 3 is a block diagram showing a brightness correction circuit 60 of the display device of Fig. 2, the circuit 60 being for blue LEDs and a brightness correction circuit for red LEDs being not shown for the sake of simplicity of the drawing;
Fig. 4 shows a format of data stored in a ROM 64 and RAM 67 of the circuit of Fig. 3;
Fig. 5 shows the details of a display panel 1 of the display device of Fig. 2;
Fig. 6 shows a data output circuit 3 and scan circuit 2 of the display device of Fig. 2;
Fig. 7 is a time chart explaining the operation of the brightness correction circuit of Fig. 3;
Fig. 8 is a time chart explaining the operation of the display device of Fig. 2; and
Fig. 9 is a time chart explaining the operation of the display device under a two-phase clock mode.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Various embodiments of the present invention will be described with reference to the accompanying drawings. It is to be noted that the same or similar reference numerals are applied to the same or similar parts and elements throughout the drawings, and the description of the same or similar parts and elements will be omitted or simplified.

Figure 2 is a block diagram showing a dot-matrix LED display device employing red and green LEDs according to an embodiment of the present invention. The display device has a main circuit 50 and a brightness correction circuit 60 connected to an input end of the main circuit 50. The brightness correction circuit 60 corrects the brightness of each of the LEDs that form a display panel 1 of the main circuit 50. The LED array 1 has a matrix of, for example, 32 x 32 of red and green LEDs 1a. The main circuit 50 also has a matrix driver unit and a control unit 4 for controlling the matrix driver unit to selectively light the red and green LEDs 1a. The matrix driver unit has a scan circuit 2 for sequentially scanning the LEDs 1a, and a data output circuit 3 for driving the LEDs 1a in synchronization with the scan timing of the scan circuit 2.

The control unit 4 has input terminals 4a for brightness-corrected 8-bit red data BRA to BRH, input terminals 4b for brightness-corrected 8-bit green data BGA to BGH, input terminals 4c for clock signals CK1 and CK2, an input terminal 4d for a reset signal RE, an input terminal 4e for a select signal SE, an input terminal 4f for a brightness signal BR, and an input terminal 4g for an oscillation pulse OSC. These input terminals 4a to 4g are connected to an output end of the brightness correction circuit 60. The input terminals 4c for the clock signals CK1 and CK2 are connected to a clock selector 5. In response to a control signal from a switch 6, the clock selector 5 selects the clock signal CK1 to achieve a one-phase clock mode or the clock signals CK1 and CK2 to achieve a two-phase clock mode. In the following explanation, the one-phase clock mode is mainly described, and the two-phase clock mode is briefly described lastly.

Figures 7 and 8 show the operation of the display device. The clock signal CK1 provides pulse groups each containing 32 pulses. An interval between the last pulse of a given pulse group and the first pulse of the next pulse group defines a lighting time. Each scanning operation covers 16 LEDs. The timing charts of Figs. 7 and 8 will be explained later in detail. Returning to Fig. 2, the LED array 1 is divided into an upper screen and a lower screen. The upper screen includes the first to 16th rows of the LED matrix, and the lower screen includes the 17th to 32nd rows thereof. The rows of LEDs are scanned one after another in each of the upper and lower screens. Each scanning operation is carried out on 16 LEDs, i.e., every LED in each row is scanned in synchronization with the clock signal CK1. This means that each row of the LED array 1 is lighted once per 16 scanning operations, i.e., at a duty factor of 1/16. A row x (x being one of 1 to 16) in the display panel 1 is lighted between pulses n and n+1 of the clock signal CK1, in which n is expressed as follows:

$$n = 32 \times (16 \times a + x)$$

where a is one of 0 to "N - 1" and N is the number of scanning operations necessary for refreshing the LED array 1 once. As shown in Fig. 8, a displaying operation is carried out between pulses n and n+1 of the clock signal CK1. Namely, a displaying operation is carried out between pulses 32 and 33, between pulses 64 and 65, ..., and between pulses 992 and 993 of the clock signal CK1.

The output of the clock selector 5 is connected to a data input control circuit 7, which is connected to brightness-corrected red and green data RAMs 8 and 9. The data input control circuit 7 is connected to the brightness data input terminals 4a and 4b and select signal input terminal 4e. The data input control circuit 7 receives

brightness-corrected red and green data in synchronization with the clock signal CK1, and provides the RAMs 8 and 9 with the respective brightness-corrected data when the select signal SE is at high level H. The outputs of the RAMs 8 and 9 are connected to gradation control circuits 10 and 11, which are connected to the data output circuit 3.

The brightness signal input terminal 4f and oscillation pulse input terminal 4g are connected to a gradation time detector 12. The brightness signal BR is used to further adjust a lighting time between pulses n and n+1 of the clock signal CK1. The gradation time detector 12 receives the oscillation pulse OSC, divides the lighting time by 256 according to the brightness signal, and calculates a gradation time. An external switch 14 and brightness adjuster 15 are used to control a surface brightness correction circuit 13. According to a value set through the brightness adjuster 15, the surface brightness correction circuit 13 provides data to correct the total brightness of the LED array 1. The gradation control circuits 10 and 11 refer to the gradation time from the gradation time detector 12 and the data from the surface brightness correction circuit 13, to control the lighting time of each LED so that the LED may display one of 256 gradation levels according to the brightness-corrected data.

The output of the clock selector 5 is connected to a two-stage 4-bit counter 17 and a two-stage 4-bit counter 18 connected in series. The outputs of the two-stage 4-bit counter 18 are connected to a two-stage decoder 19, which is connected to the scan circuit 2. The reset signal input terminal 4d is connected to the clock selector 5, surface brightness correction circuit 13, and 4-bit counters 17 and 18 so that the reset signal RE may reset these circuits. The control unit 4 has a power source terminal Vcc1 and a ground terminal GND1, and a matrix driver unit has a power source terminal Vcc2 and a ground terminal GND2.

Figure 3 is a block diagram showing the details of the brightness correction circuit 60. This circuit is for red LEDs. For the sake of simplicity of explanation, a brightness correction circuit for green LEDs is omitted. Accordingly, the circuit 60 of Fig. 3 receives only external red display data RA to RH. The brightness correction circuit 60 has a counter 61 for counting the number of the oscillation pulses OSC, a counter 62 for counting the reset signals RE, and a counter 63 for counting pulses of the clock signal CK1. The counters 61 and 62 are connected to selectors 64 and 65, respectively. The selector 64 selects the output of the counter 61 or the oscillation pulse OSC according to the select signal SE. The selector 65 selects the output of the counter 62 or the reset signal RE according to the select signal SE. The output of the selector 64 is connected to the counter 66, and the output of the selector 65 is supplied as a reset signal to the counter 66. The output of the counter 66 is supplied to an input terminal of an address selector 67, and as an address of the ROM 69 to store brightness-corrected data, to the buffer 68.

Ten-bit output data of the counter 63 and the external 8-bit gradation data, i.e., red display data RA to RH are supplied to the other input terminal of the address selector 67. The output of the address selector 67 is supplied as an address of a RAM 71 to a buffer 70. The output of the selector 64 is supplied to the buffer 68 and a clock selector 72. If the output of the selector 64 is selected by the clock selector 72, it will be an enable signal EB to the buffer 70. The clock selector 72 also receives the clock signal CK1. If the clock signal CK1 is selected by the clock selector 72, it will be an enable signal EB to the buffer 70.

The select signal SE controls the data output of the counters 66 and 63, the selection operation of the address selector 67, the selection operation of the clock selector 72, the read (R)/write (W) operation of the RAM 71, and the read operation of the ROM 69. A read terminal of the RAM 71 receives the select signal SE through an inverter 73. The counter 63 is reset by the select signal SE. The output side of the ROM 69 is connected to the input/output side of the RAM 71. The brightness-corrected data from the RAM 71 is sent to the input terminals 4a of the main circuit 50 through an output buffer 74. The clock signal CK1 is passed through a buffer 75 and the output buffer 74 and is supplied to the input terminal 4c of the main circuit 50. The reset signal RE, select signal SE, brightness signal BR, and oscillation pulse OSC are supplied to the input terminals 4d, 4e, 4f, and 4g, respectively, through the output buffer 74.

Figure 4 shows a format of data stored in the ROM 69 and RAM 71. The ROM 69 stores the brightness-corrected data of each LED at a corresponding address. The address of each LED is 10-bit data (= 32 x 32 LEDs), and the brightness (gradation) data of each LED is 8-bit data, as shown in Fig. 4. According to this embodiment, the ROM 69 and RAM 71 employing the format of Fig. 4 are required for each of red and green LED groups.

Figure 5 shows the detail of the LED array 1 of Fig. 2. The display panel 1 has a matrix of 32 data lines s1 to s32 and 32 scan lines p1 to p32 with the LEDs 1a being connected to the intersections of the data and scan lines. Two sets (not shown) of the matrix of 32 data lines and 32 scan lines of Fig. 5 are arranged for the red and green LED groups, respectively.

Figure 6A shows a unit structure of the data output circuit 3 and Fig. 6B shows a unit structure of the scan circuit 2 of Fig. 2. The unit data output circuit 3 of Fig. 6A has an input inverter 31, two bipolar transistors 32 and 33, and resistors 34, 35, and 36. This unit structure is for one data line. Namely, there are 32 unit structures for the 32 data lines. When an input terminal 30 receives display data of low level, the output of the inverter 31 supplies a base current to the NPN transistor 32 through the resistor 34, to turn ON the NPN transistor 32. As a result, a current from a power source flows through the resistors 36 and 35 and NPN transistor 32, to turn ON the PNP transistor 33. Then, an output terminal 37 connected to, for example, the data line s1 of the LED array 1 becomes high level, to activate the data line s1.

The unit scan circuit 2 of Fig. 6B has two bipolar transistors 41 and 42 and two resistors 43 and 44. This unit structure is for one scan line. Namely, there are 32 unit structures for the 32 scan lines. When an input terminal 40 receives a signal of high level, a base current is supplied to the NPN transistor 41 through the resistor 43, to turn ON the NPN transistor 41. As a result, a current from a power source flows through the resistor 44 and NPN transistor 41 to the base of the NPN transistor 42, to turn ON the NPN transistor 42. Then, an output terminal 45 connected to, for example, the scan line p1 of the LED array 1 becomes low level, to activate the scan line p1. Consequently, the LED 1a connected to the data line s1 and scan line p1 emits light.

The operation of the dot-matrix LED display device and a method of adjusting the brightness of the same will be explained with reference to the time charts of Figs. 7 and 8. The brightness of each LED of the LED array 1 is measured by a brightness measurement device, and according to the measured brightness, brightness-corrected data to minimize brightness difference among LEDs is prepared for every LED of the LED array 1. The prepared brightness-corrected data is stored in the ROM 69 in the format of Fig. 4.

The operation of the brightness correction circuit 60 will be explained with reference to the time chart of Fig. 7.

The clock signal CK1 according to the embodiment intermittently provides 32 pulse groups each containing 32 pulses. Namely, the clock signal CK1 repeatedly provides 1024 (= 32 x 32) pulses. When the select signal SE is being at low level up to time t1, the address selector 67 selects the counter 66, the clock selector 72 selects the output of the selector 64, the RAM 71 is put in a write mode, and the counter 66 and ROM 69 are enabled. As a result, the output of the counter 66 is supplied as an address of the ROM 69 to the buffer 68, to transfer corresponding brightness-corrected data from the ROM 69 to the RAM 71. When the select signal SE becomes high level after the time t1, the counter 66 is stopped, the address selector 67 selects the counter 63 and display data RA to RH, the clock selector 72 selects the clock signal CK1, and the RAM 71 is put in a read mode. As a result, the brightness-corrected data stored in the RAM 71 addressed by the 18-bit output data of the address selector 67 is sent to the input terminals 4a of the main circuit 50 in synchronization with the clock signal CK1. This operation is continued up to time t2 up to which the select signal SE is kept at high level.

Figure 8 shows the displaying operation of the main circuit 50 while the select signal SE is being at high level. The brightness-corrected data BRA to BRH and BGA to BGH are supplied to the input terminals 4a and 4b of the main circuit 50. A pulse of the reset signal RE is supplied at time t11, and the select signal SE and brightness signal BR successively become high level at time t12 and t13. At time t14, a first pulse of a first pulse group of the clock signal CK1 rises. In synchronization with 32 pulses of the first pulse group of the clock signal CK1, brightness-corrected data S1 for 32 LEDs in the first row of the display panel 1 is stored in the RAMs 8 and 9 through the data input control circuit 7. While the brightness signal BR is being at high level from time t13 to t15, the displaying operation is OFF.

Thereafter, the brightness signal BR is kept at low level from time t15 to t16 during which the brightness-corrected data S1 stored this scanning operation is read for 16 LEDs in the first row of the LED array 1, and brightness-corrected data S17 stored at the previous scanning operation is read for 16 LEDs in the 17th row of the LED array 1, out of the RAMs 8 and 9. The read data are supplied to the gradation control circuits 10 and 11. The gradation control circuits 10 and 11 determine the lighting time of each of these LEDs in the first and 17th rows according to the read brightness-corrected data S1 and S17, a gradation time divided by 256 provided by the gradation time detector 12, and data from the surface brightness correction circuit 13. Then, these LEDs are lighted at specified gradation levels.

During a period between time t16 and t17, the same process as that in the period between time t14 and t15 is carried out, and brightness-corrected data S2 for the second row of the LED array 1 is read. In the next period up to time t18, the brightness-corrected data S2 for the second row and brightness-corrected data S18 for the 18th row are used to display each 16 LEDs in the second and 18th rows, similar to the period between time t15 and t16. In this way, brightness-corrected data S3 to S32 for the third to 32nd rows are read, and each 16 LEDs of the upper and lower screens of the display panel 1 are lighted.

To transfer the brightness-corrected data from the ROM 69 to the RAM 71, 2^{18} pulses of the clock signal CK1 are needed. In this case, 2^{18} is nearly equal to 262^{k}. If a standard VGA (Video Graphic Adaptor) mode (640 x 480 dots) for a CRT is employed for the dot-matrix LED display device of this embodiment, the frequency of the clock signal CK1 will be about 25 MHz. According to the VGA mode, the number of dot clock pulses between pulses of a horizontal synchronous signal is 800, and the number of pulses of the horizontal synchronous signal between pulses of a vertical synchronous signal is 525. Accordingly, if the frequency of the oscillation pulse OSC is about 10 MHz, the following expression is made:

$$800 \times 525 = 420000 = 420^{k}$$

Since one screen involves 420^{k} pulses, the brightness-corrected data in the RAM may be refreshed once per two frames. If the frequency of the oscillation pulse OSC is equal to the frequency of the clock signal CK1, the data in the RAM may be refreshed every screen.

In this way, the embodiment of the present invention provides brightness-corrected data from the RAM while the select signal SE being at high level. Namely, the RAM provides corresponding brightness-corrected data according to an address of display data, and the LEDs on the LED array are driven according to the brightness-corrected data. The lighting time of each LED on the LED

array is determined according to the brightness-corrected data that is specified by the address of the LED. Even if there is brightness difference among LEDs of an LED array due to fluctuations in the characteristics of the LEDs, the present invention prepares brightness-corrected data for the LEDs to minimize the brightness differences. The brightness-corrected data is read according to externally provided display data. With this arrangement, the display device will be of low cost and high quality.

The present invention is not limited to the embodiment mentioned above. Various modifications are possible over the embodiment. For example, instead of red and green LEDs, red, green, and blue LEDs may be employed to display a full-color image on the display device. The full-color display device comprises matrixes of AlGaAs red LEDs, GaP or InGaAlP green LEDs, GaN or ZnSe blue LEDs. The main circuit 50 shown in Fig. 2 may have a matrix driver unit and a control unit 4 for selectively light the red, green and blue LEDs. The control unit 4 shown in Fig. 2 may have input terminals for brightness-corrected 8-bit red data BRA to BRH, input terminals 4b for brightness-corrected 8-bit green data BGA to BGH, and input terminals 4z for brightness-corrected 8-bit blue data BBA to BBH. And the full-color display device include the brightness correction circuits 60 for red, green and blue LEDs. As to Fig. 5, three sets of the matrix are arranged for the red, green and blue LED groups, respectively. And the brightness-corrected data BRA to BRH, BGA to BGH and BBA to BBH are supplied to the input terminals of the main circuit 50 shown in Fig. 2. The brightness-corrected red, green and blue data are stored in the RAM 71 of Fig. 3 and transferred to the RAMs 8 and 9.

In the above embodiment, brightness-corrected data is stored in the RAM 71 of Fig. 3 firstly, and when the select signal SE is at high level, the brightness-corrected data is transferred from the RAM 71 to the RAMs 8 and 9 of Fig. 2. Instead, the RAM 71 may hold display data, which is always provided as an address for the RAMs 8 and 9, which store the brightness-corrected data.

The brightness-corrected data may be converted into an analog voltage, which is supplied to the input terminal 30 of the data output circuit 3 to drive the LEDs.

The above explanation has been made for the one-phase clock mode. The two-phase clock mode will be carried out similarly according to a time chart shown in Fig. 9. By the two-phase clock mode, the faster scanning operation is possible than the one-phase clock mode. The one-phase clock mode and two-phase clock mode are switched from one to another by providing the clock selector 5 of Fig. 2 with a control signal from the switch 6.

Claims

1. An LED display device comprising an LED array with a dot matrix of LEDs, a matrix driver unit for driving the LEDs, a control unit for controlling the matrix driver unit, and a brightness correction circuit having a data storage unit for storing brightness-corrected data for each of the LEDs to minimize brightness difference among the LEDs,

   wherein the brightness-corrected data is selected according to externally provided display data, to drive the control unit.

2. A device as claimed in claim 1, in which said LED array includes dot matrixes of red, green and blue LEDs, and said brightness correction circuit includes circuits for the red, green and blue LEDs, so that brightness-corrected red, green and blue data is selected to drive the control unit.

3. An LED display device comprising:

   (a) an LED array with a dot matrix of LEDs;
   (b) a matrix driver unit for driving the LEDs;
   (c) a control unit for controlling the matrix driver unit;
   (d) a ROM for storing brightness-corrected data prepared according to the characteristic brightness of each of the LEDs to minimize brightness difference among the LEDs; and
   (e) a RAM connected to said ROM and the control unit, for storing the brightness-corrected data held in said ROM,

   wherein the brightness-corrected data is transferred from said ROM to said RAM when no display data is externally provided, and the brightness-corrected data stored in said RAM is selected according to externally provided display data, to drive the control unit.

4. A device as claimed in claim 3, in which said LED array includes dot matrixes of red, green and blue LEDs, so that brightness-corrected red, green and blue data are transferred from said ROM to said RAM.

5. An LED display device comprising:

   (a) an LED array with a dot matrix of LEDs;
   (b) a matrix driver unit for driving the LEDs;
   (c) a control unit having a first RAM for holding data to drive the LEDs, to control the matrix driver unit according to the data in the first RAM;
   (d) a ROM for storing brightness-corrected data prepared according to the characteristic brightness of each of the LEDs to minimize brightness difference among the LEDs; and
   (e) a second RAM connected to said ROM and the control unit, addressed according to externally provided display data to provide output data,

   wherein the brightness-corrected data is transferred from said ROM to said second RAM when no display data is externally provided, and

the first RAM stores the transferred brightness-corrected data to drive the LEDs.

6. A device as claimed in claim 1, 3 or 5, in which the display data is gradation data represented with a plurality of bits.

7. A device as claimed in claim 1, 3 or 5, in which the control unit has a gradation time detection circuit and a surface brightness correction circuit, and the lighting time of each of the LEDs is determined according to a gradation time calculated by the gradation time detection circuit, data provided by the surface brightness correction circuit, and the brightness-corrected data.

8. A device as claimed in claim 5, in which said LED array includes dot matrixes of red, green and blue LEDs, so that brightness-corrected red, green and blue data are transferred from said ROM to said second RAM, and said first RAM stores the brightness-corrected red, green and blue data to drive the LEDs.

9. A brightness control method for an LED display device having an LED array with a dot matrix of LEDs, a matrix driver unit for driving the LEDs, a control unit for controlling the matrix driver unit, and a data storage unit, which comprises:

(a) preparing brightness-corrected data according to the characteristic brightness of each of the LEDs to minimize brightness difference among the LEDs;
(b) storing the brightness-corrected data in a data storage unit; and
(c) selecting the brightness-corrected data stored in the data storage unit according to externally provided display data, and driving the LEDs according to the selected brightness-corrected data.

10. A method as claimed in claim 9, in which said LED array includes dot matrixes of red, green and blue LEDs, so that brightness-corrected red, green and blue data are prepared, stored and selected.

FIG. 1

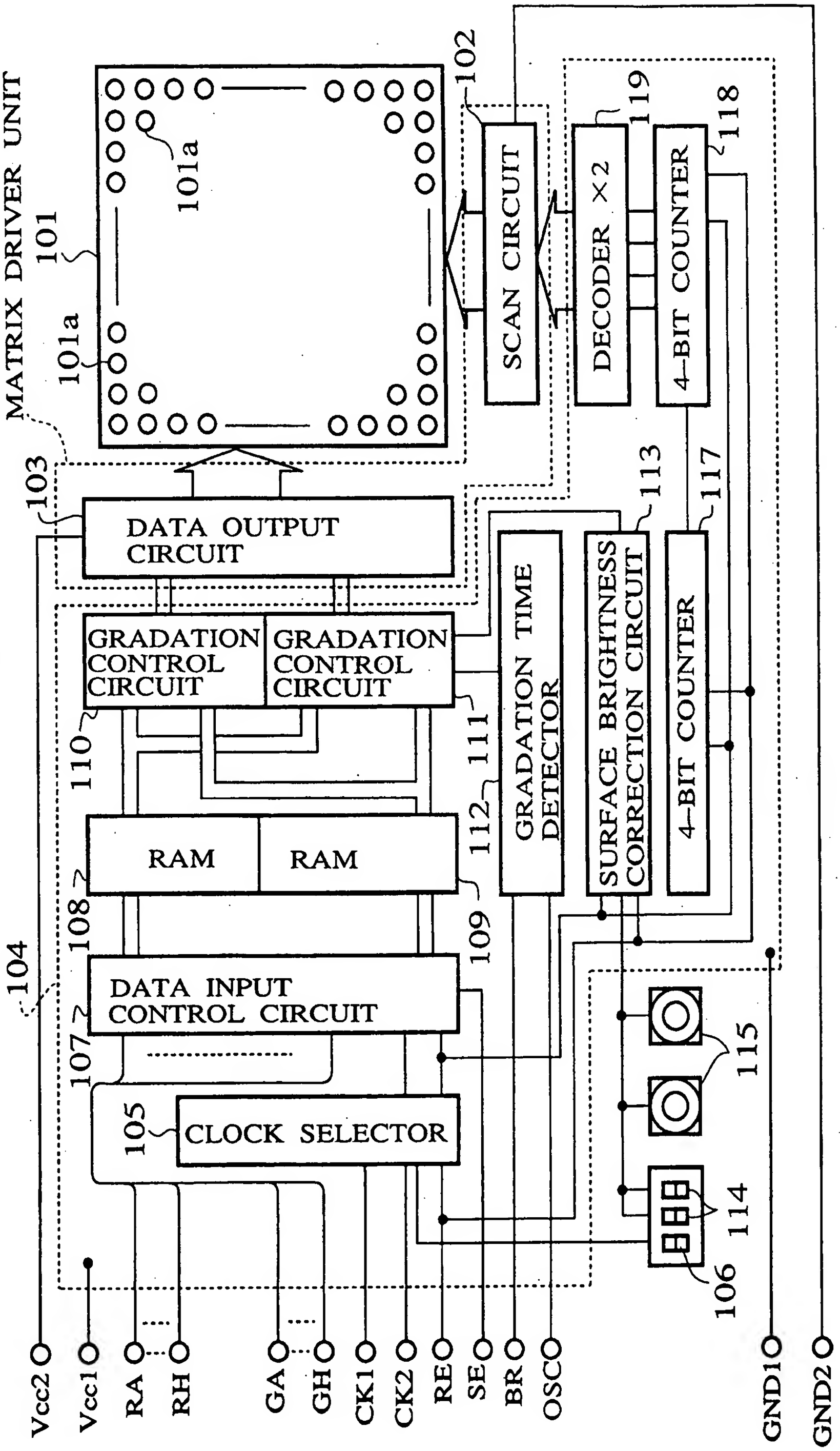
MATRIX DRIVER UNIT
101
101a
101a
102
SCAN CIRCUIT
DECODER ×2
119
4-BIT COUNTER
118
103
DATA OUTPUT CIRCUIT
GRADATION CONTROL CIRCUIT
GRADATION CONTROL CIRCUIT
110
111
GRADATION TIME DETECTOR
112
SURFACE BRIGHTNESS CORRECTION CIRCUIT
113
4-BIT COUNTER
117
RAM
RAM
108
109
104
DATA INPUT CONTROL CIRCUIT
107
105
CLOCK SELECTOR
115
114
106
Vcc2
Vcc1
RA
RH
GA
GH
CK1
CK2
RE
SE
BR
OSC
GND1
GND2

FIG.2

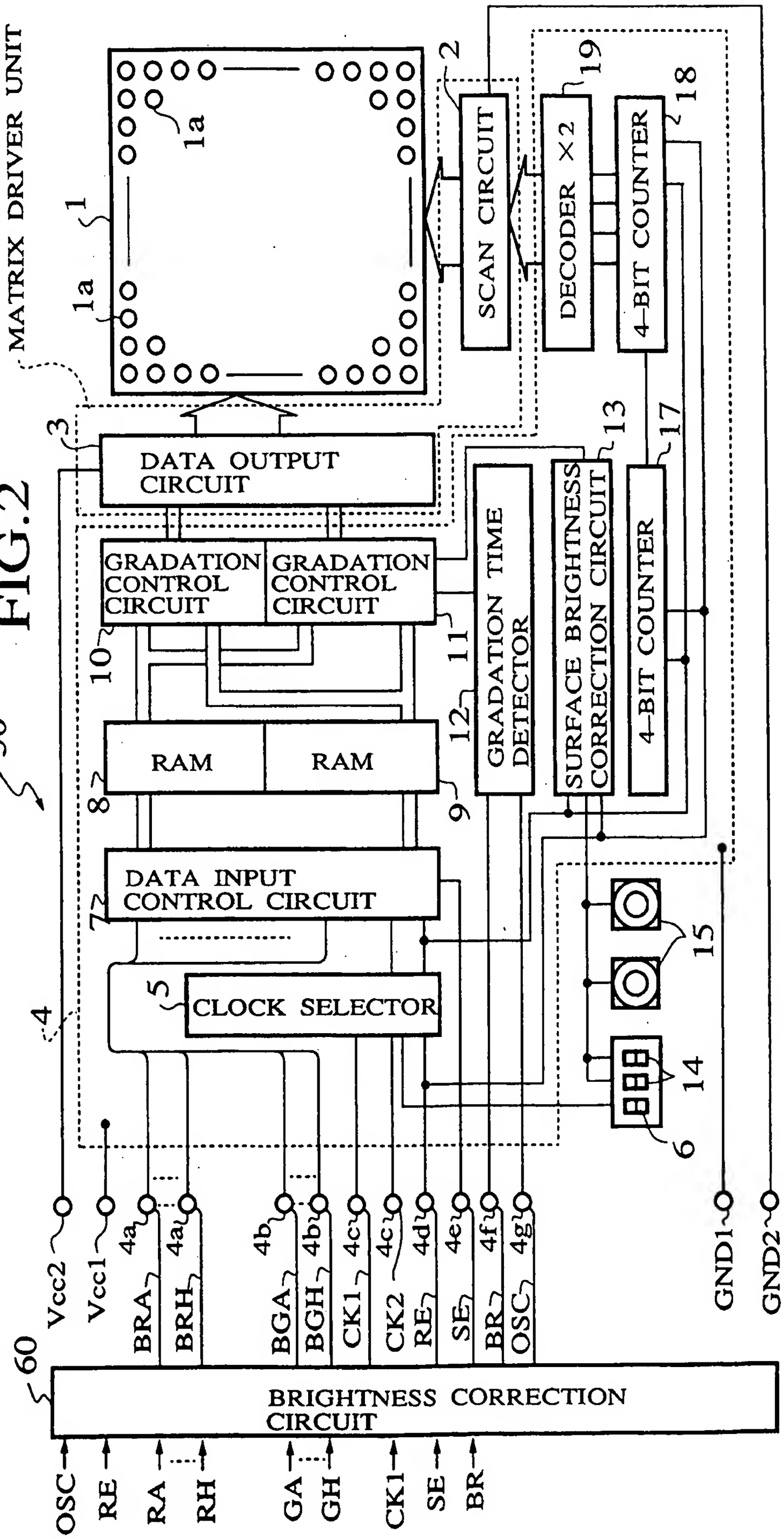
MATRIX DRIVER UNIT
1
1a
1a
2
SCAN CIRCUIT
DECODER ×2
19
4-BIT COUNTER
18
3
DATA OUTPUT CIRCUIT
13
17
GRADATION CONTROL CIRCUIT
GRADATION CONTROL CIRCUIT
10
11
GRADATION TIME DETECTOR
SURFACE BRIGHTNESS CORRECTION CIRCUIT
4-BIT COUNTER
50
12
RAM
RAM
8
9
DATA INPUT CONTROL CIRCUIT
7
15
5
CLOCK SELECTOR
4
14
6
Vcc2
Vcc1
4a
BRA
4a
BRH
4b
BGA
4b
BGH
4c
CK1
4c
CK2
4d
RE
4e
SE
4f
BR
4g
OSC
GND1
GND2
60
BRIGHTNESS CORRECTION CIRCUIT
OSC
RE
RA
RH
GA
GH
CK1
SE
BR

FIG.3

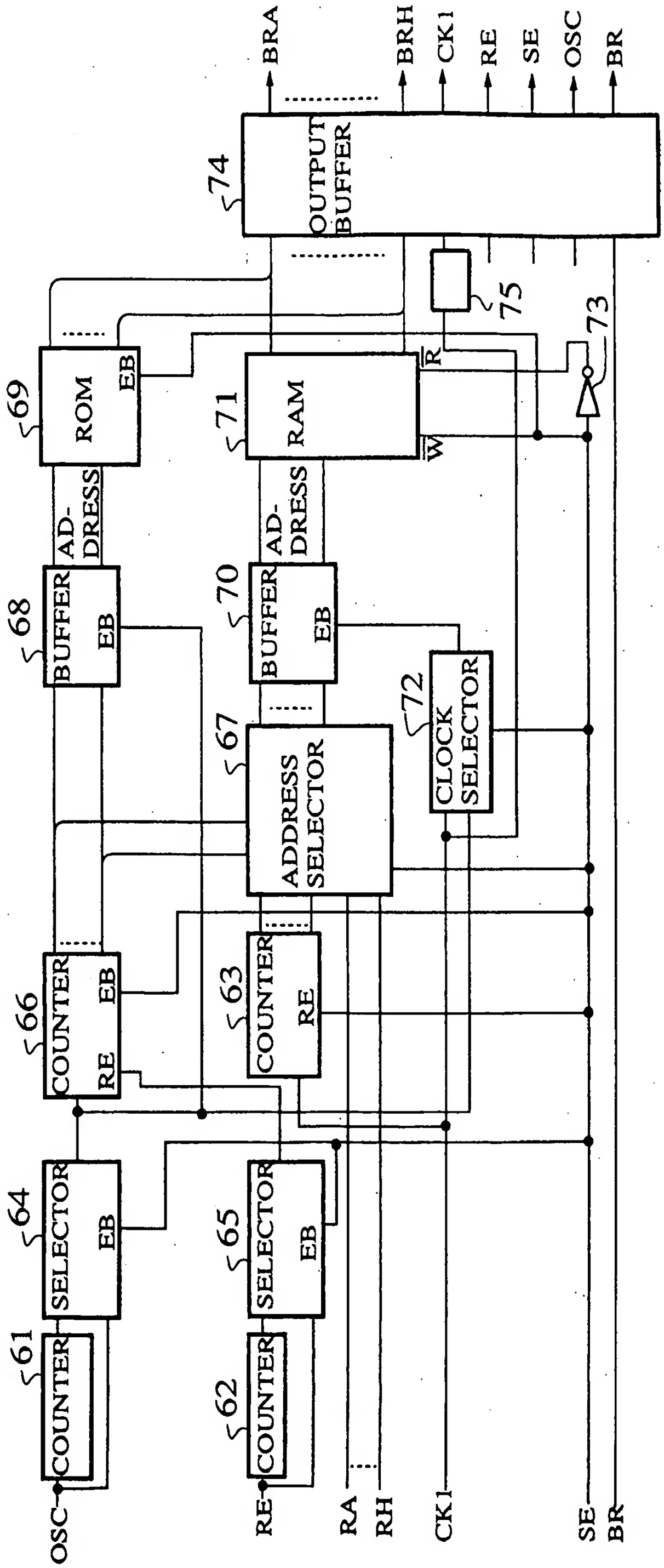
BRA
BRH
CK1
RE
SE
OSC
BR
74
OUTPUT BUFFER
75
73
69
ROM
EB
71
RAM
R
W
AD-DRESS
68
BUFFER
EB
70
BUFFER
EB
67
ADDRESS SELECTOR
72
CLOCK SELECTOR
66
COUNTER
EB
RE
63
COUNTER
RE
64
SELECTOR
EB
65
SELECTOR
EB
61
COUNTER
62
COUNTER
OSC
RE
RA
RH
CK1
SE
BR

FIG.4

DATA	ADDRESS		CORRESPONDING DOT
	DOT POSITION ON DISPLAY PANEL	8-BIT INPUT DATA	
00000010	00000000	00000000	(1, 1)
00000001	00000001	00000001	(1, 2)
00000000	00000010	00000010	(1, 3)
00000000	00000011	00000011	(1, 4)
00000000	00000100	00000100	(1, 5)
00000000	00000101	00000101	(1, 6)
00000000	00000110	00000110	(1, 7)
00000000	00000111	00000111	(1, 8)
00000000	00001000	00001000	(2, 1)
00000000	00001001	00001001	(2, 2)
00000000	00001010	00001010	(2, 3)
00000000	00001011	00001011	(2, 4)
00000000	00001100	00001100	(2, 5)
00000000	00001101	00001101	(2, 6)
00000000	00001110	00001110	(2, 7)
00000000	00001111	00001111	(2, 8)
00000000	00010000	00010000	(3, 1)
00000000	00010001	00010001	(3, 2)
00000000	00010010	00010010	(3, 3)
00000000	00010011	00010011	(3, 4)
00000000	00010100	00010100	(3, 5)
00000000	00010101	00010101	(3, 6)
00000000	00010110	00010110	(3, 7)
00000000	00010111	00010111	(3, 8)
00000000	00011000	00011000	(4, 1)
00000000	00011001	00011001	(4, 2)
00000000	00011010	00011010	(4, 3)
00000000	00011011	00011011	(4, 4)
00000000	00011100	00011100	(4, 5)
00000000	00011101	00011101	(4, 6)
00000000	00011110	00011110	(4, 7)
00000000	00011111	00011111	(4, 8)
00000000	00100000	00100000	(5, 1)
00000000	00100001	00100001	(5, 2)
00000000	00100010	00100010	(5, 3)
00000000	00100011	00100011	(5, 4)
00000000	00100100	00100100	(5, 5)
00000000	00100101	00100101	(5, 6)
00000000	00100110	00100110	(5, 7)
00000000	00100111	00100111	(5, 8)
00000000	00101000	00101000	(6, 1)
00000000	00101001	00101001	(6, 2)
00000000	00101010	00101010	(6, 3)
00000000	00101011	00101011	(6, 4)
00000000	00101100	00101100	(6, 5)
00000000	00101101	00101101	(6, 6)
00000000	00101110	00101110	(6, 7)
00000000	00101111	00101111	(6, 8)
00000000	00110000	00110000	(7, 1)
00000000	00110001	00110001	(7, 2)
00000000	00110010	00110010	(7, 3)
00000000	00110011	00110011	(7, 4)
00000000	00110100	00110100	(7, 5)
00000000	00110101	00110101	(7, 6)
00000000	00110110	00110110	(7, 7)
00000000	00110111	00110111	(7, 8)
00000000	00111000	00111000	(8, 1)
00000000	00111001	00111001	(8, 2)
00000000	00111010	00111010	(8, 3)
00000000	00111011	00111011	(8, 4)
00000000	00111100	00111100	(8, 5)
00000000	00111101	00111101	(8, 6)
00000000	00111110	00111110	(8, 7)
00000000	00111111	00111111	(8, 8)
00000000	01000000	01000000	(9, 1)
00000000	01000001	01000001	(9, 2)
00000000	01000010	01000010	(9, 3)
00000000	01000011	01000011	(9, 4)
00000000	01000100	01000100	(9, 5)
00000000	01000101	01000101	(9, 6)
00000000	01000110	01000110	(9, 7)
00000000	01000111	01000111	(9, 8)
00000000	01001000	01001000	(10, 1)
00000000	01001001	01001001	(10, 2)
00000000	01001010	01001010	(10, 3)
00000000	01001011	01001011	(10, 4)
00000000	01001100	01001100	(10, 5)
00000000	01001101	01001101	(10, 6)
00000000	01001110	01001110	(10, 7)
00000000	01001111	01001111	(10, 8)
00000000	01010000	01010000	(11, 1)
00000000	01010001	01010001	(11, 2)
00000000	01010010	01010010	(11, 3)
00000000	01010011	01010011	(11, 4)
00000000	01010100	01010100	(11, 5)
00000000	01010101	01010101	(11, 6)
00000000	01010110	01010110	(11, 7)
00000000	01010111	01010111	(11, 8)
00000000	01011000	01011000	(12, 1)
00000000	01011001	01011001	(12, 2)
00000000	01011010	01011010	(12, 3)
00000000	01011011	01011011	(12, 4)
00000000	01011100	01011100	(12, 5)
00000000	01011101	01011101	(12, 6)
00000000	01011110	01011110	(12, 7)
00000000	01011111	01011111	(12, 8)
00000000	01100000	01100000	(13, 1)
00000000	01100001	01100001	(13, 2)
00000000	01100010	01100010	(13, 3)
00000000	01100011	01100011	(13, 4)
00000000	01100100	01100100	(13, 5)
00000000	01100101	01100101	(13, 6)
00000000	01100110	01100110	(13, 7)
00000000	01100111	01100111	(13, 8)
00000000	01101000	01101000	(14, 1)
00000000	01101001	01101001	(14, 2)
00000000	01101010	01101010	(14, 3)
00000000	01101011	01101011	(14, 4)
00000000	01101100	01101100	(14, 5)
00000000	01101101	01101101	(14, 6)
00000000	01101110	01101110	(14, 7)
00000000	01101111	01101111	(14, 8)
00000000	01110000	01110000	(15, 1)
00000000	01110001	01110001	(15, 2)
00000000	01110010	01110010	(15, 3)
00000000	01110011	01110011	(15, 4)
00000000	01110100	01110100	(15, 5)
00000000	01110101	01110101	(15, 6)
00000000	01110110	01110110	(15, 7)
00000000	01110111	01110111	(15, 8)
00000000	01111000	01111000	(16, 1)
00000000	01111001	01111001	(16, 2)
00000000	01111010	01111010	(16, 3)
00000000	01111011	01111011	(16, 4)
00000000	01111100	01111100	(16, 5)
00000000	01111101	01111101	(16, 6)
00000000	01111110	01111110	(16, 7)
00000000	01111111	01111111	(16, 8)
00000000	10000000	10000000	(17, 1)
00000000	10000001	10000001	(17, 2)
00000000	10000010	10000010	(17, 3)
00000000	10000011	10000011	(17, 4)
00000000	10000100	10000100	(17, 5)
00000000	10000101	10000101	(17, 6)
00000000	10000110	10000110	(17, 7)
00000000	10000111	10000111	(17, 8)
00000000	10001000	10001000	(18, 1)
00000000	10001001	10001001	(18, 2)
00000000	10001010	10001010	(18, 3)
00000000	10001011	10001011	(18, 4)
00000000	10001100	10001100	(18, 5)
00000000	10001101	10001101	(18, 6)
00000000	10001110	10001110	(18, 7)
00000000	10001111	10001111	(18, 8)
00000000	10010000	10010000	(19, 1)
00000000	10010001	10010001	(19, 2)
00000000	10010010	10010010	(19, 3)
00000000	10010011	10010011	(19, 4)
00000000	10010100	10010100	(19, 5)
00000000	10010101	10010101	(19, 6)
00000000	10010110	10010110	(19, 7)
00000000	10010111	10010111	(19, 8)
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00000000	10011001	10011001	(20, 2)
00000000	10011010	10011010	(20, 3)
00000000	10011011	10011011	(20, 4)
00000000	10011100	10011100	(20, 5)
00000000	10011101	10011101	(20, 6)
00000000	10011110	10011110	(20, 7)
00000000	10011111	10011111	(20, 8)
00000000	10100000	10100000	(21, 1)
00000000	10100001	10100001	(21, 2)
00000000	10100010	10100010	(21, 3)
00000000	10100011	10100011	(21, 4)
00000000	10100100	10100100	(21, 5)
00000000	10100101	10100101	(21, 6)
00000000	10100110	10100110	(21, 7)
00000000	10100111	10100111	(21, 8)
00000000	10101000	10101000	(22, 1)
00000000	10101001	10101001	(22, 2)
00000000	10101010	10101010	(22, 3)
00000000	10101011	10101011	(22, 4)
00000000	10101100	10101100	(22, 5)
00000000	10101101	10101101	(22, 6)
00000000	10101110	10101110	(22, 7)
00000000	10101111	10101111	(22, 8)
00000000	10110000	10110000	(23, 1)
00000000	10110001	10110001	(23, 2)
00000000	10110010	10110010	(23, 3)
00000000	10110011	10110011	(23, 4)
00000000	10110100	10110100	(23, 5)
00000000	10110101	10110101	(23, 6)
00000000	10110110	10110110	(23, 7)
00000000	10110111	10110111	(23, 8)
00000000	10111000	10111000	(24, 1)
00000000	10111001	10111001	(24, 2)
00000000	10111010	10111010	(24, 3)
00000000	10111011	10111011	(24, 4)
00000000	10111100	10111100	(24, 5)
00000000	10111101	10111101	(24, 6)
00000000	10111110	10111110	(24, 7)
00000000	10111111	10111111	(24, 8)
00000000	11000000	11000000	(25, 1)
00000000	11000001	11000001	(25, 2)
00000000	11000010	11000010	(25, 3)
00000000	11000011	11000011	(25, 4)
00000000	11000100	11000100	(25, 5)
00000000	11000101	11000101	(25, 6)
00000000	11000110	11000110	(25, 7)
00000000	11000111	11000111	(25, 8)
00000000	11001000	11001000	(26, 1)
00000000	11001001	11001001	(26, 2)
00000000	11001010	11001010	(26, 3)
00000000	11001011	11001011	(26, 4)
00000000	11001100	11001100	(26, 5)
00000000	11001101	11001101	(26, 6)
00000000	11001110	11001110	(26, 7)
00000000	11001111	11001111	(26, 8)
00000000	11010000	11010000	(27, 1)
00000000	11010001	11010001	(27, 2)
00000000	11010010	11010010	(27, 3)
00000000	11010011	11010011	(27, 4)
00000000	11010100	11010100	(27, 5)
00000000	11010101	11010101	(27, 6)
00000000	11010110	11010110	(27, 7)
00000000	11010111	11010111	(27, 8)
00000000	11011000	11011000	(28, 1)
00000000	11011001	11011001	(28, 2)
00000000	11011010	11011010	(28, 3)
00000000	11011011	11011011	(28, 4)
00000000	11011100	11011100	(28, 5)
00000000	11011101	11011101	(28, 6)
00000000	11011110	11011110	(28, 7)
00000000	11011111	11011111	(28, 8)
00000000	11100000	11100000	(29, 1)
00000000	11100001	11100001	(29, 2)
00000000	11100010	11100010	(29, 3)
00000000	11100011	11100011	(29, 4)
00000000	11100100	11100100	(29, 5)
00000000	11100101	11100101	(29, 6)
00000000	11100110	11100110	(29, 7)
00000000	11100111	11100111	(29, 8)
00000000	11101000	11101000	(30, 1)
00000000	11101001	11101001	(30, 2)
00000000	11101010	11101010	(30, 3)
00000000	11101011	11101011	(30, 4)
00000000	11101100	11101100	(30, 5)
00000000	11101101	11101101	(30, 6)
00000000	11101110	11101110	(30, 7)
00000000	11101111	11101111	(30, 8)
00000000	11110000	11110000	(31, 1)
00000000	11110001	11110001	(31, 2)
00000000	11110010	11110010	(31, 3)
00000000	11110011	11110011	(31, 4)
00000000	11110100	11110100	(31, 5)
00000000	11110101	11110101	(31, 6)
00000000	11110110	11110110	(31, 7)
00000000	11110111	11110111	(31, 8)
00000000	11111000	11111000	(32, 1)
00000000	11111001	11111001	(32, 2)
00000000	11111010	11111010	(32, 3)
00000000	11111011	11111011	(32, 4)
00000000	11111100	11111100	(32, 5)
00000000	11111101	11111101	(32, 6)
00000000	11111110	11111110	(32, 7)
00000000	11111111	11111111	(32, 8)

FIG.5

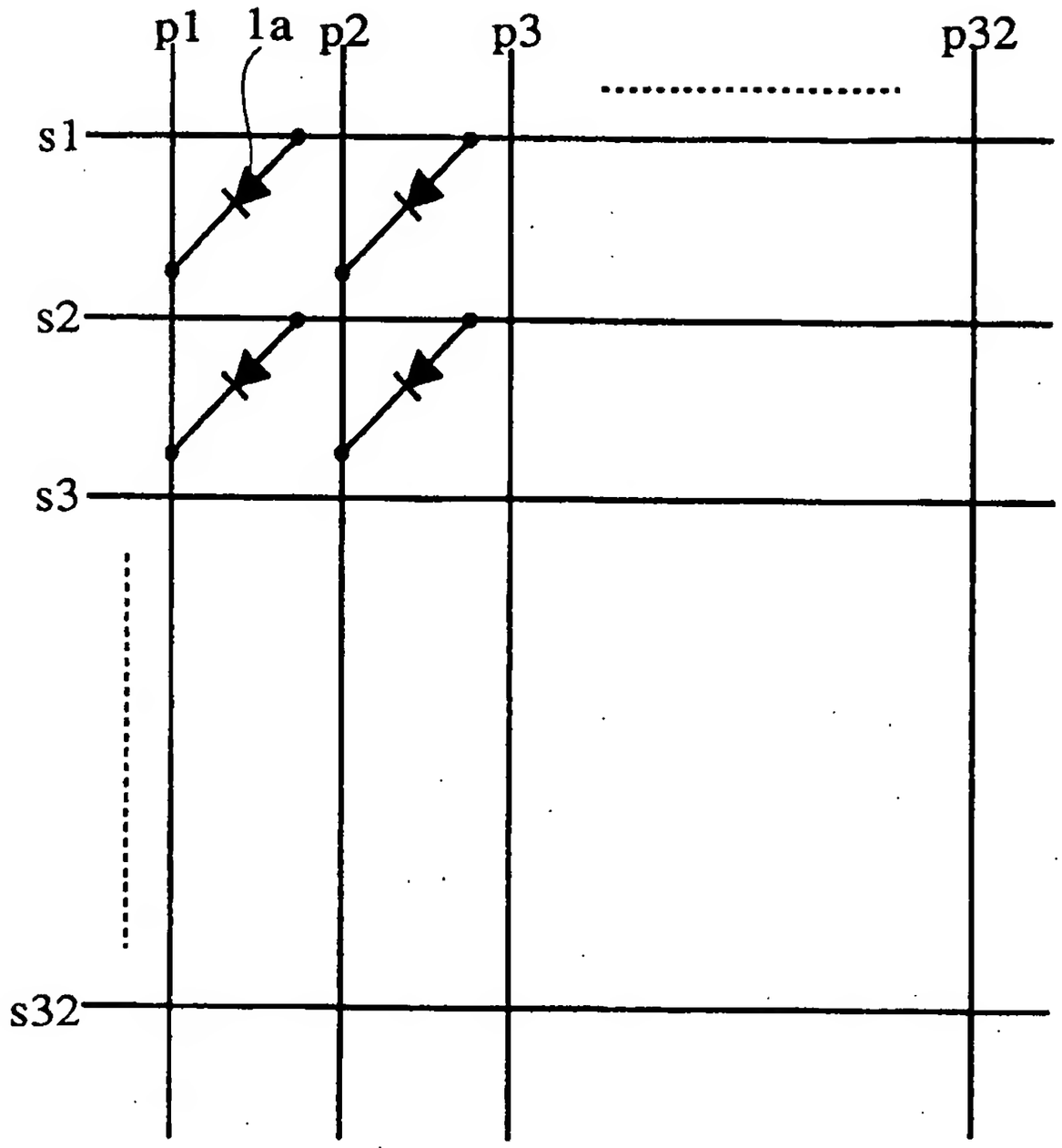


FIG.6A

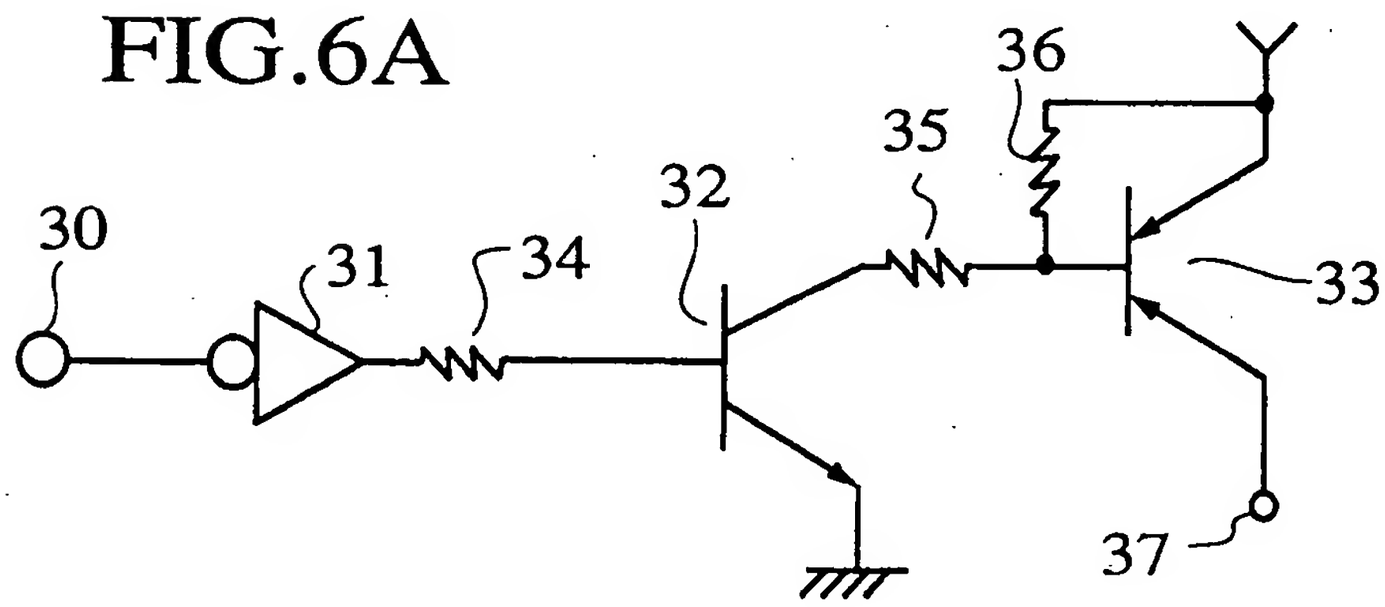


FIG.6B

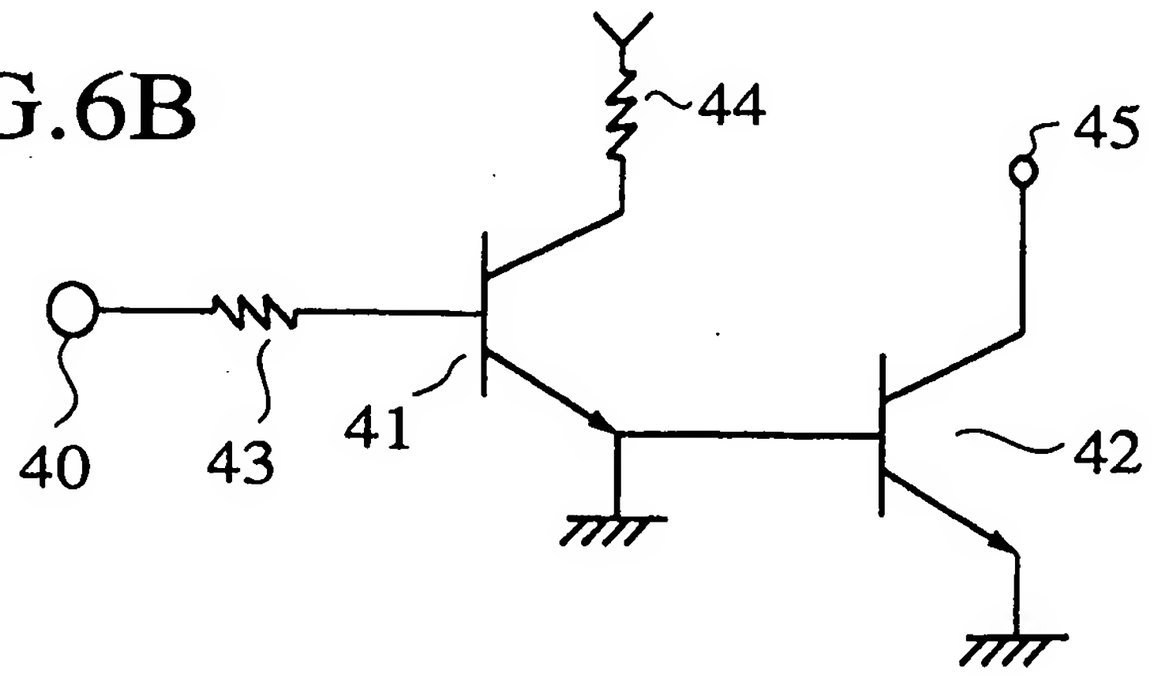


FIG.7

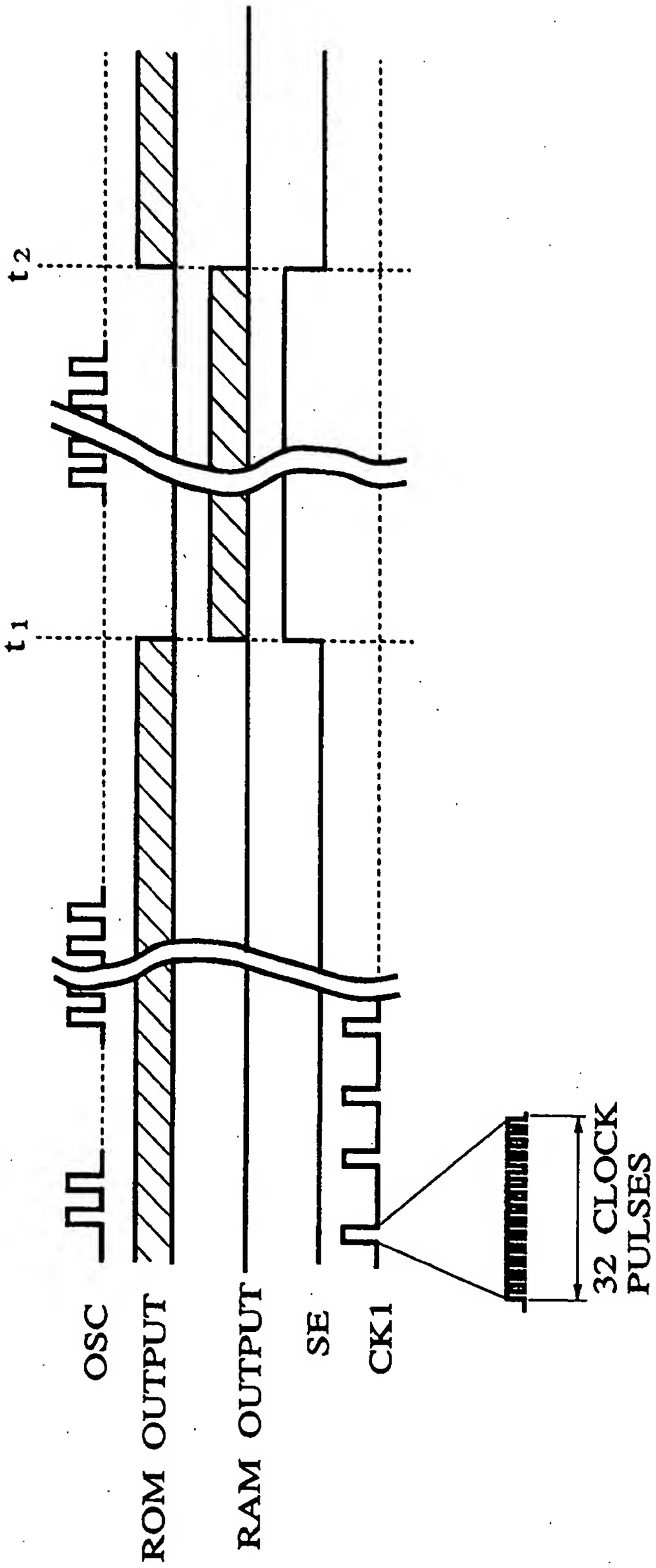


FIG.8

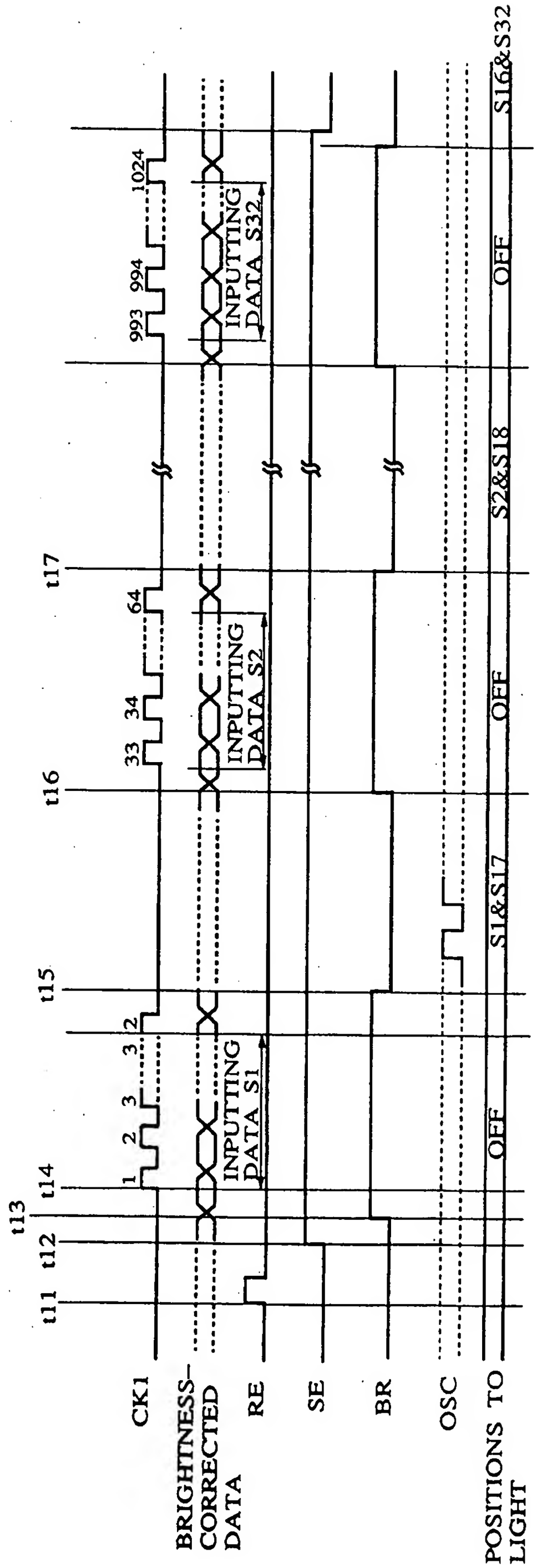
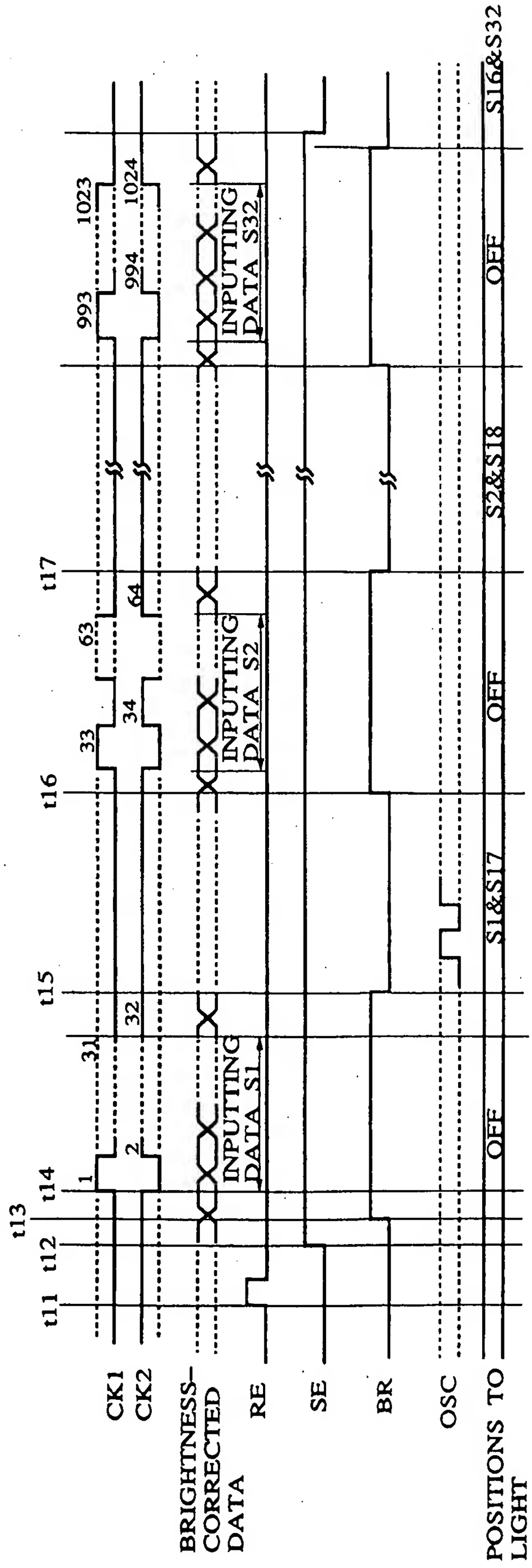

CK1
BRIGHTNESS-CORRECTED DATA
RE
SE
BR
OSC
POSITIONS TO LIGHT
t11
t12
t13
t14
t15
t16
t17
1
2
3
INPUTTING DATA S1
OFF
33
34
64
INPUTTING DATA S2
OFF
993
994
1024
INPUTTING DATA S32
OFF
S1&S17
S2&S18
S16&S32

FIG.9


t11
t12
t13
t14
t15
t16
t17
CK1
CK2
BRIGHTNESS-CORRECTED DATA
RE
SE
BR
OSC
POSITIONS TO LIGHT
1
2
31
32
33
34
63
64
993
994
1023
1024
INPUTTING DATA S1
INPUTTING DATA S2
INPUTTING DATA S32
OFF
S1&S17
S2&S18
S16&S32

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 11 1247

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 18 no. 50 (P-1683) ,26 January 1994 & JP-A-05 273939 (SHARP CO.) 22 October 1993,	1,2,9,10	G09G3/32
A	* abstract *	3,5	
Y	GB-A-2 176 042 (INTEGRATED SYSTEMS ENGINEERING INC.) * page 4, line 112 - line 121 * * figure 11 *	1,2,9,10	
Y	FR-A-2 683 365 (RAYTHEON CO.) * page 20, line 17 - page 21, line 8 * * page 27, line 15 - line 31 * * page 28, line 28 - page 31, line 13 * * figures 4,9 *	1,2,9,10	
A	GB-A-2 210 720 (CHENG) * abstract *	1,3,5,9	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 November 1995	Farricella, L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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